WHAT IS CLAIMED IS:

1. An electrostatic discharge protection circuit, connecting a bonding pad and a pre-stage device, comprising:

a P-type metal-oxide semiconductor (PMOS) transistor, comprising a first source/drain region, a second source/drain region and a gate electrode, wherein the first source/drain region of the PMOS transistor is connected to a system power source, and the gate electrode is connected to the pre-stage device, and the second source/drain region of the PMOS transistor is connected to the bonding pad;

an N-type metal-oxide semiconductor (NMOS) transistor, comprising a first source/drain region, a second source/drain region and a gate electrode, wherein the first source/drain region of the NMOS transistor is connected to the second source/drain region of the PMOS transistor and the bonding pad, the second source/drain region of the NMOS transistor is grounded, and the gate electrode of the NMOS receives an output from the pre-stage device; and

a capacitor, connecting to the source/drain region of the PMOS transistor, which is also connected to the system power source, and the gate electrode of the NMOS transistor.

2. The circuit claimed as claim 1, wherein the pre-stage device comprises a pre-stage driving device.

3. An electrostatic discharge protection circuit, connecting to a bonding pad and a pre-stage device, the electrostatic discharge protection circuit comprising:

a first P-type metal-oxide semiconductor (PMOS) transistor, comprising a first source/drain region, a second source/drain region and a gate electrode, wherein the first source/drain region of the PMOS is connected to a system power source, and the gate

electrode is connected to the pre-stage device, and the second source/drain region of the PMOS is connected to the bonding pad;

a first N-type metal-oxide semiconductor (NMOS) transistor, comprising first source/drain region, a second source/drain region and a gate electrode, wherein the first source/drain region of the first NMOS transistor is connected to the bonding pad, and the gate electrode is connected to the system power source;

a second NMOS transistor having a first source/drain region, a second source/drain region and a gate electrode, wherein the first source/drain region of the second NMOS is connected to the second source/drain region of the first NMOS transistor, and the second source/drain region of the second NMOS transistor is connected to the grounded node, and the gate electrode of the second NMOS transistor receives an output of the pre-stage device;

a capacitor; and

a second PMOS transistor having a first source/drain region, a second source/drain region and a gate electrode, wherein the capacitor is connected between the first source/drain region of the second PMOS transistor and a substrate of the first PMOS transistor, and the gate electrode of the second PMOS transistor is connected to the system power source, the second source/drain region of the second PMOS transistor is connected to the gate electrode of the second NMOS transistor, and receives the output of the pre-stage device.

4. The circuit claimed as claim 3, wherein the capacitor comprises a metal-oxide semiconductor capacitor.

5. The circuit claimed as claim 4, wherein the metal-oxide semiconductor (MOS) capacitor comprises a MOS transistor having two source/drain regions and a substrate

that connect together to serve as a first electrode of the MOS capacitor, and a gate electrode of the MOS transistor serves as a second electrode of the MOS capacitor.

6. The circuit claimed as claim 3, comprising a third PMOS transistor having a first and second source/drain regions and a gate electrode, wherein the first source/drain region of the third PMOS transistor is connected to the system power source, the gate electrode is grounded, and the second source/drain region of the third PMOS transistor is connected between the capacitor and the first source/drain region of the second PMOS transistor.

7. The method claimed as claim 3, wherein the pre-stage device comprises a pre-stage driver.